



Description

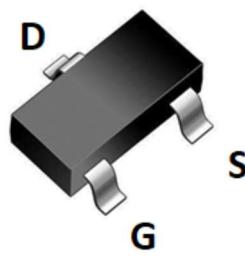
JMD N-channel Depletion Mode Power MOSFET

Features

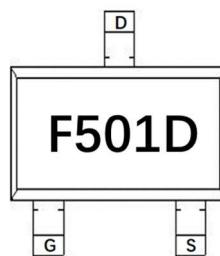
- 600V, 0.03A
- $R_{DS(ON)} < 700\Omega$ @ $V_{GS} = 0V$
- $R_{DS(ON)} < 800\Omega$ @ $V_{GS} = 10V$
- Self-aligned planner technology
- Pb-free lead plating
- Halogen free
- ESD improved capability

Application

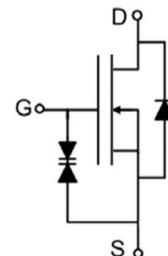
- Load Switch
- PWM Application
- Power management



SOT-23 top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
F501D	JMDL501A	TAPING	SOT-23	7inch	3000	180000

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		600	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current		$T_A = 25^\circ C$	A
			$T_A = 100^\circ C$	A
I_{DM}	Pulsed Drain Current ^{note1}		0.12	A
dv/dt	Peak Diode Recovery dv/dt		5.0	V/ns
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5k Ω)		300	V
P_D	Power Dissipation	$T_A = 25^\circ C$	0.5	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		250	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS} = -5\text{V}$, $I_D = 250\mu\text{A}$	600	-	-	V
$I_{D(\text{off})}$	Off-state Drain to Source Current	$V_{DS} = 600\text{V}$, $V_{GS} = -5\text{V}$, $T_J = 25^\circ\text{C}$	-	-	0.1	μA
		$V_{DS} = 480\text{V}$, $V_{GS} = -5\text{V}$, $T_J = 125^\circ\text{C}$	-	-	10	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
I_{DSS}	On-state drain current	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$	12	-	-	mA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = 3\text{V}$, $I_D = 8\mu\text{A}$	-2.7	-1.8	-1.0	V
$R_{DS(\text{on})}$	Static Drain-Source on-Resistance note2	$V_{GS} = 0\text{V}$, $I_D = 3\text{mA}$	-	350	700	Ω
		$V_{GS} = 10\text{V}$, $I_D = 16\text{mA}$	-	400	800	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = -5\text{V}$, $f = 1.0\text{MHz}$	-	50	-	pF
C_{oss}	Output Capacitance		-	4.53	-	pF
C_{rss}	Reverse Transfer Capacitance		-	1.08	-	pF
Q_g	Total Gate Charge	$V_{DS} = 400\text{V}$, $I_D = 0.01\text{A}$, $V_{GS} = -5\text{V}$ to 5V	-	1.14	-	nC
Q_{gs}	Gate-Source Charge		-	0.5	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	0.37	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS} = 300\text{V}$, $I_D = 0.01\text{A}$, $R_{\text{GEN}} = 6\Omega$, $V_{GS} = -5\text{V}$ to 7V	-	9.9	-	ns
t_r	Turn-on Rise Time		-	55.8	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	56.4	-	ns
t_f	Turn-off Fall Time		-	136	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	0.03	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	0.12	A	
V_{SD}	Diode Forward Voltage	$I_F = 16\text{mA}$, $V_{GS} = -5\text{V}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = -5\text{V}$, $I_F = 0.01\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$	-	243	-	ns
Q_{rr}	Reverse Recovery Charge		-	636	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

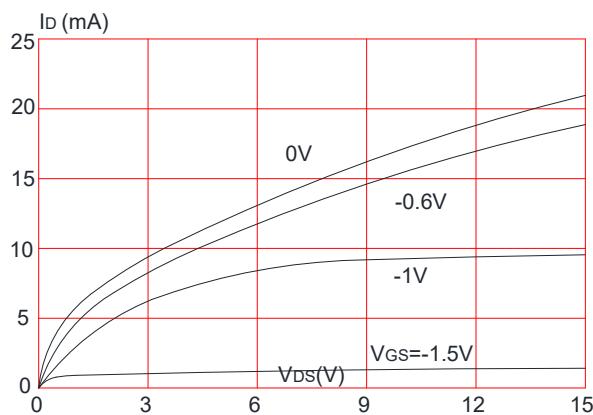
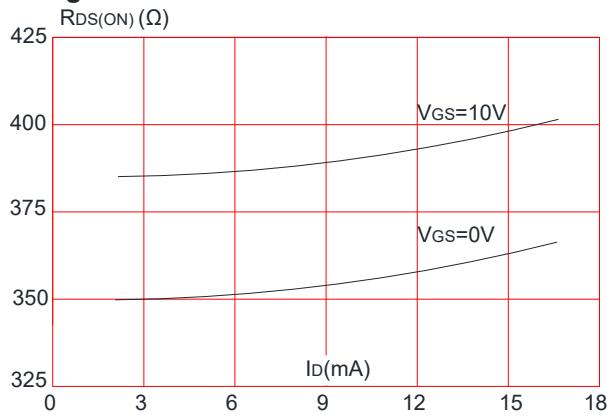
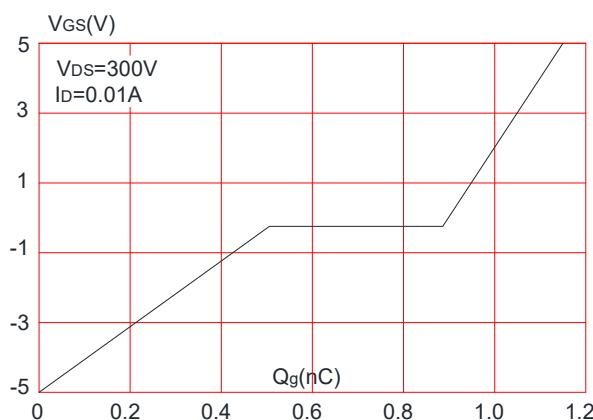
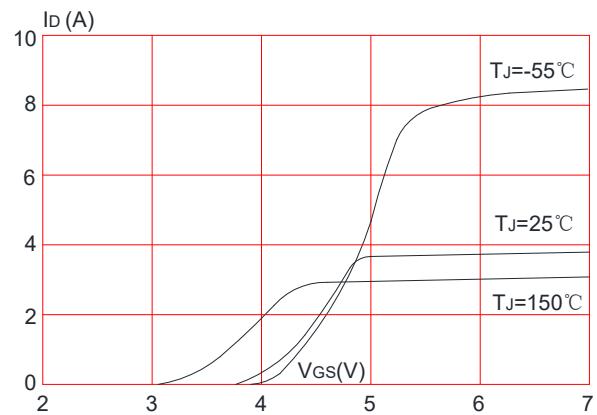
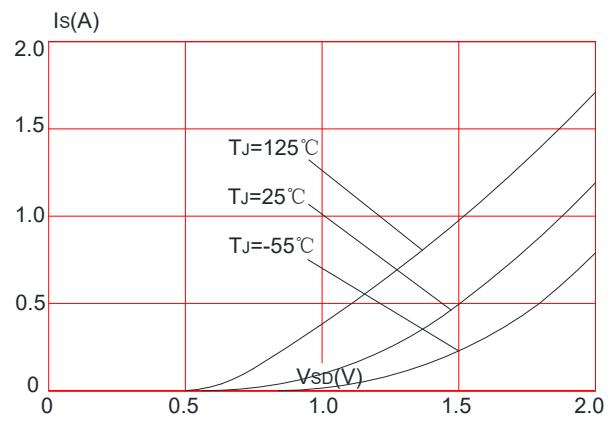
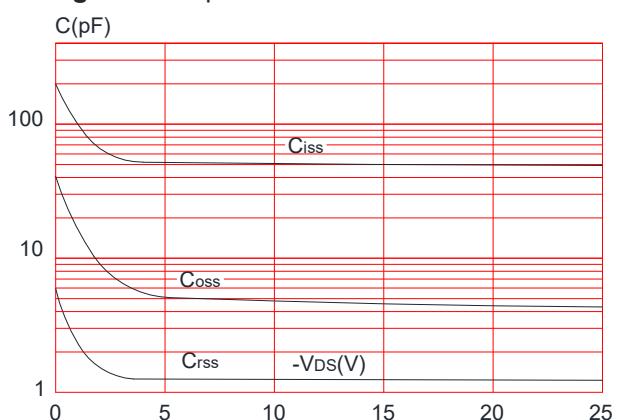
Figure1: Output Characteristics

Figure 3: On-resistance vs. Drain Current

Figure 5: Gate Charge Characteristics

Figure 2: Typical Transfer Characteristics

Figure 4: Body Diode Characteristics

Figure 6: Capacitance Characteristics


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

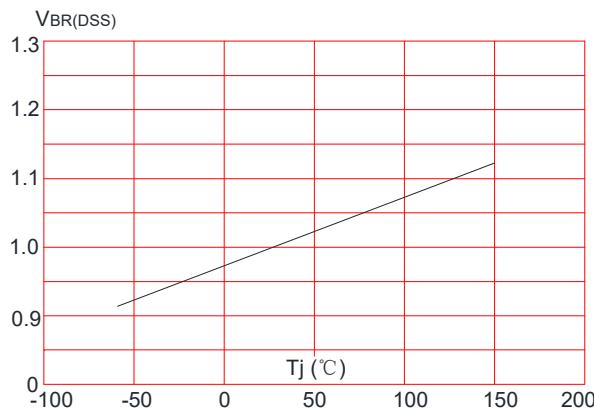


Figure 9: Maximum Safe Operating Area

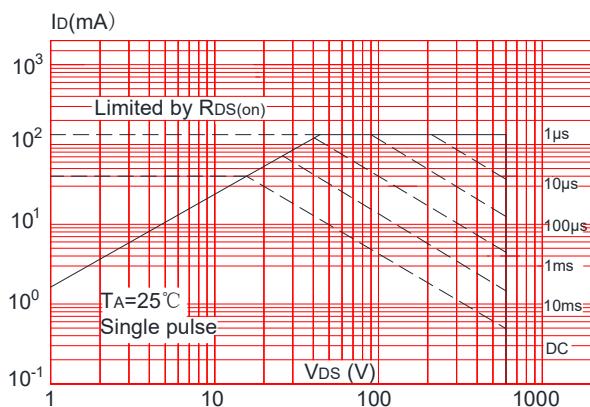


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

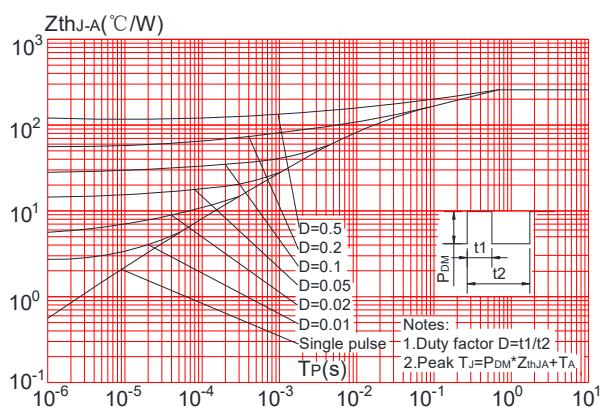


Figure 8: Normalized on Resistance vs. Junction Temperature

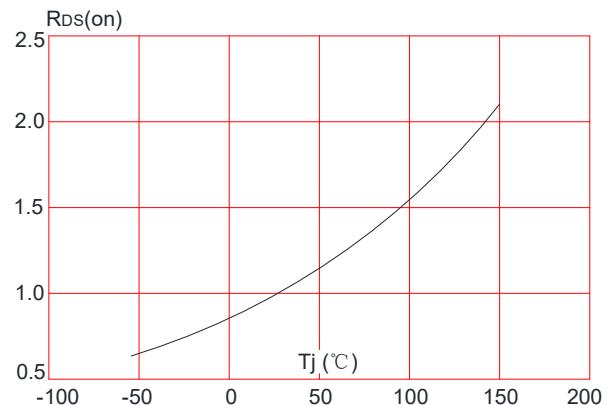
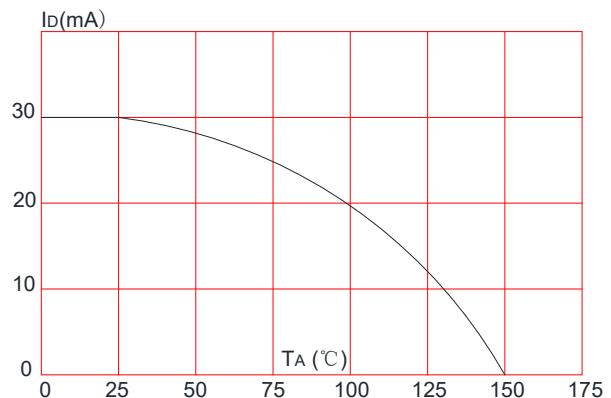


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature



Test Circuit

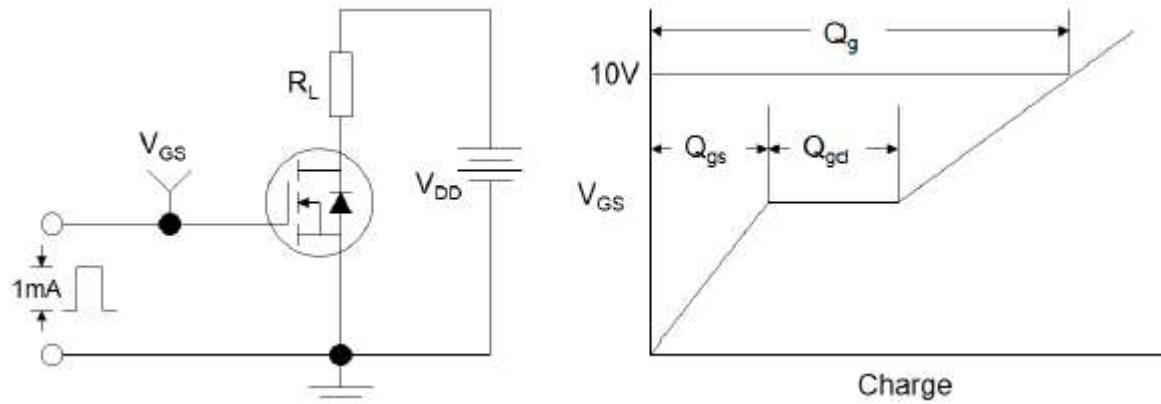


Figure1:Gate Charge Test Circuit & Waveform

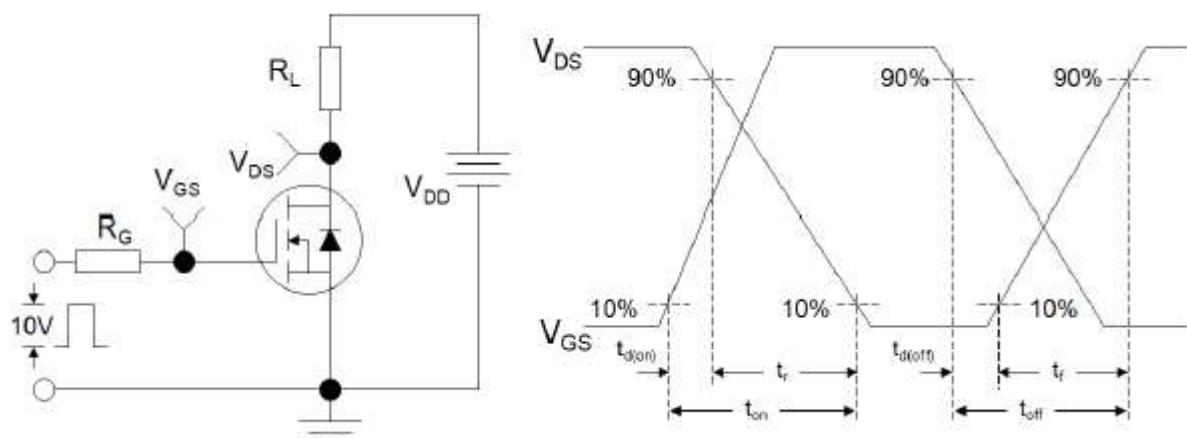


Figure 2: Resistive Switching Test Circuit & Waveforms

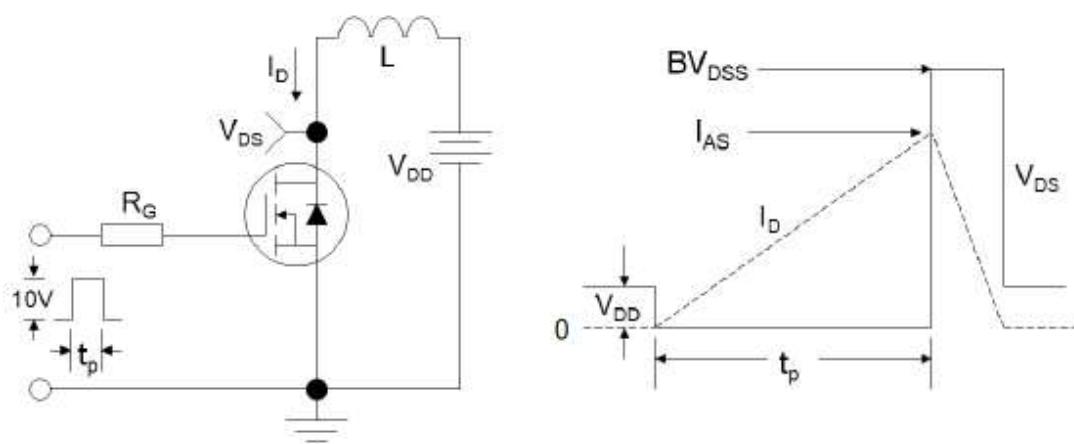
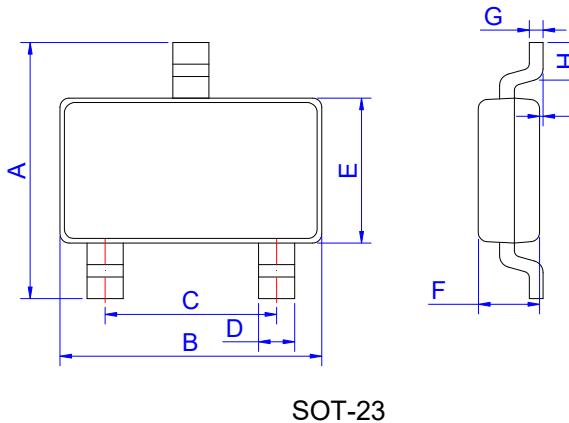


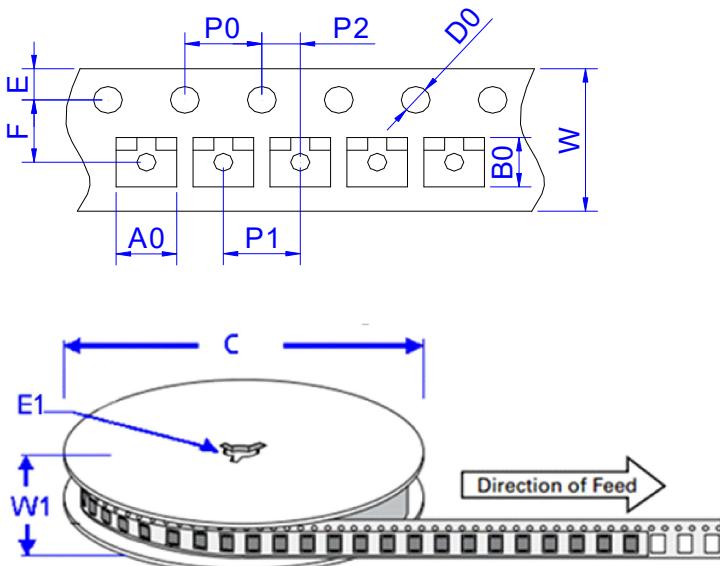
Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data-SOT-23



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.30	2.40	2.50	0.091	0.095	0.098
B	2.80	2.90	3.00	0.110	0.114	0.118
C	1.90 REF			0.075 REF		
D	0.35	0.40	0.45	0.014	0.016	0.018
E	1.20	1.30	1.40	0.047	0.051	0.055
F	0.90	1.00	1.10	0.035	0.039	0.043
G		0.10	0.15		0.004	0.006
H	0.20			0.008		
I	0		0.10	0		0.004

Package Information-SOT-23



Ref.	Dimensions	
	Millimeters	Inches
A0	3.15 ± 0.3	0.124 ± 0.012
B0	2.77 ± 0.3	0.109 ± 0.012
C	178	7.0
D0	1.50±0.1	0.059 ± 0.004
E	1.75 ± 0.2	0.069 ± 0.008
E1	13.3±0.3	0.524± 0.012
F	3.5 ± 0.2	0.138 ± 0.008
P0	4.00 ± 0.2	0.157 ± 0.008
P1	4.00 ± 0.2	0.157 ± 0.008
P2	2.00 ± 0.2	0.079 ± 0.008
W	8.00 ± 0.2	0.315 ± 0.008
W1	11.5±1.0	0.453 ± 0.039



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

JJ is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.
Copyright ©2019 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.