



Description

JMP N-channel Enhancement Mode Power MOSFET

Features

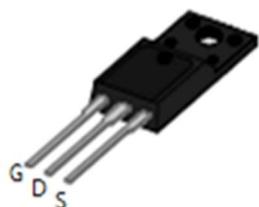
- 650V, 20A
- $R_{DS(ON)} < 0.44\Omega$ @ $V_{GS} = 10V$
- Fast Switching
- Improved dv/dt Capability

Application

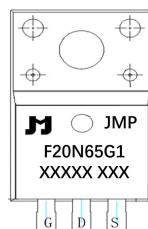
- Load Switch
- PWM Application
- Power management



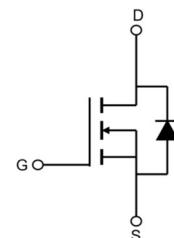
100% UIS TESTED!
100% ΔV_{ds} TESTED!



TO-220FP top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	TUBE (PCS)	Inner Box (PCS)	Per Carton (PCS)
JMPF20N65G1	JMPF20N65G1	TUBE	TO-220FP	50	1,000	5,000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		650	V
V_{GSS}	Gate-Source Voltage		± 30	V
I_D	Continuous Drain Current	$T_c = 25^\circ C$	20	A
		$T_c = 100^\circ C$	13	A
I_{DM}	Pulsed Drain Current ^{note1}		80	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		661	mJ
P_D	Power Dissipation	$T_c = 25^\circ C$	120	W
R_{eJC}	Thermal Resistance, Junction to Case		1.04	$^\circ C/W$
R_{eJA}	Thermal Resistance, Junction to Ambient		62.5	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}= \pm 30\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static Drain-Source on-Resistance note3	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$	-	0.35	0.44	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	3300	-	pF
C_{oss}	Output Capacitance		-	255	-	pF
C_{rss}	Reverse Transfer Capacitance		-	13	-	pF
Q_g	Total Gate Charge	$V_{DD}=520\text{V}$, $I_D=20\text{A}$, $V_{GS}=10\text{V}$	-	86	-	nC
Q_{gs}	Gate-Source Charge		-	16	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	36	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-on Delay Time	$V_{DD}=325\text{V}$, $I_D=20\text{A}$, $R_G=25\Omega$	-	37	-	ns
t_r	Turn-on Rise Time		-	66	-	ns
$t_{d(\text{off})}$	Turn-off Delay Time		-	175	-	ns
t_f	Turn-off Fall Time		-	84	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	20	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	80	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_{SD}=20\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS}=0\text{V}$, $I_s=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	450	-	ns
Q_{rr}	Reverse Recovery Charge		-	7.1	-	μC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $V_G = 10\text{V}$, $L = 10\text{mH}$, $I_{AS} = 11.5\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

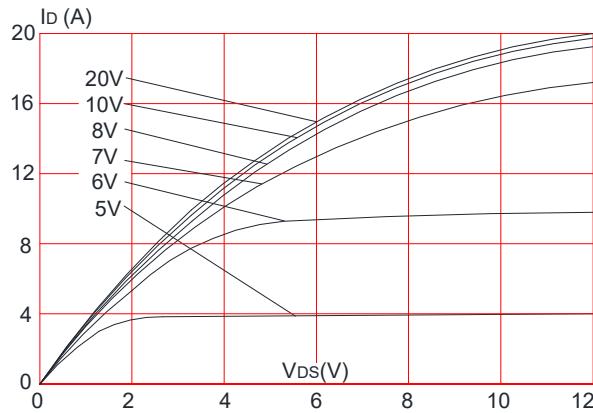


Figure 3: On-resistance vs. Drain Current

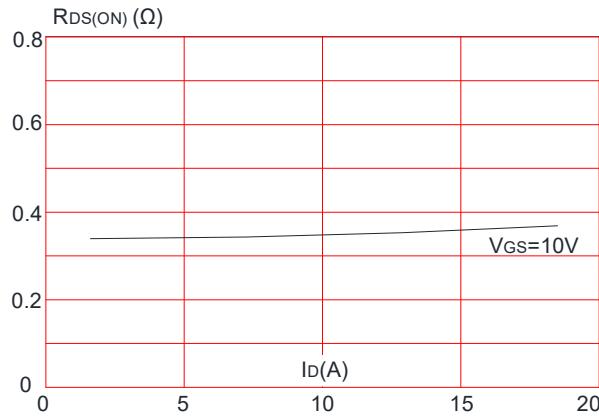


Figure 5: Gate Charge Characteristics

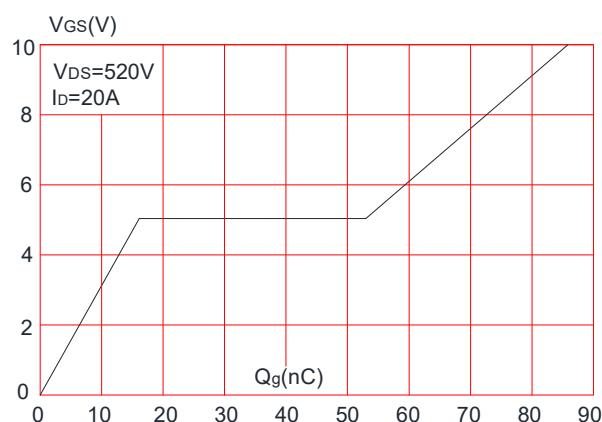


Figure 2: Typical Transfer Characteristics

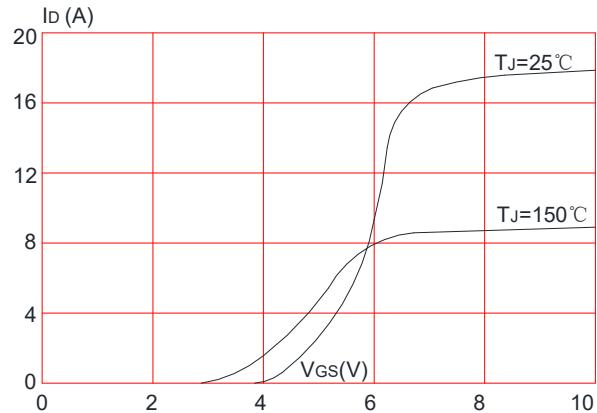


Figure 4: Body Diode Characteristics

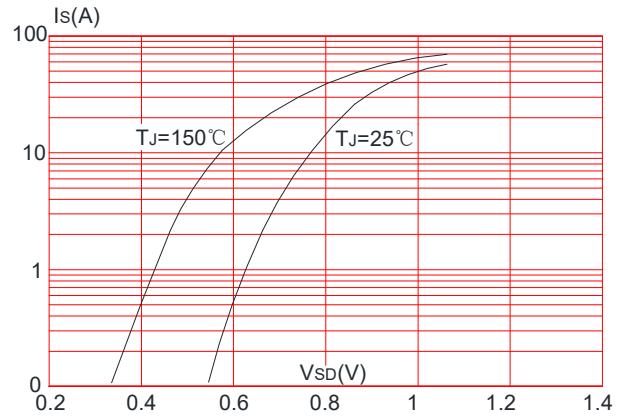


Figure 6: Capacitance Characteristics

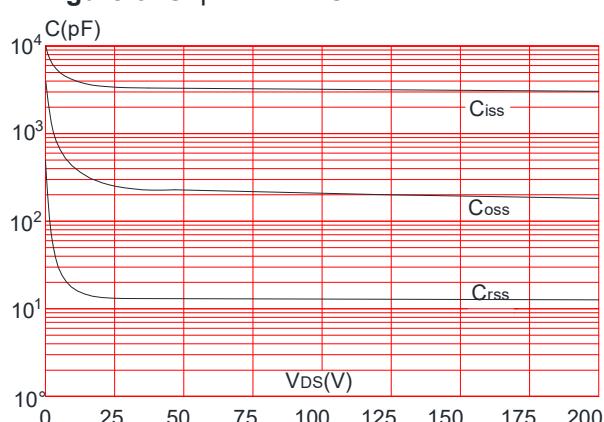


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

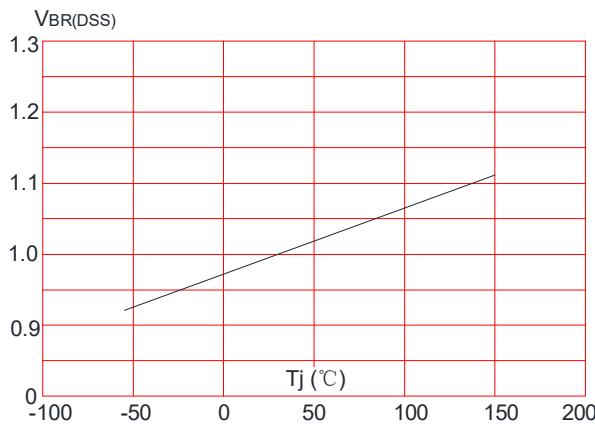


Figure 8: Normalized on Resistance vs. Junction Temperature

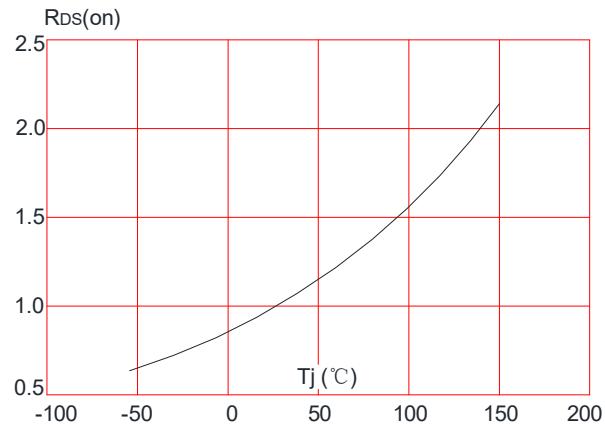


Figure 9: Maximum Safe Operating Area

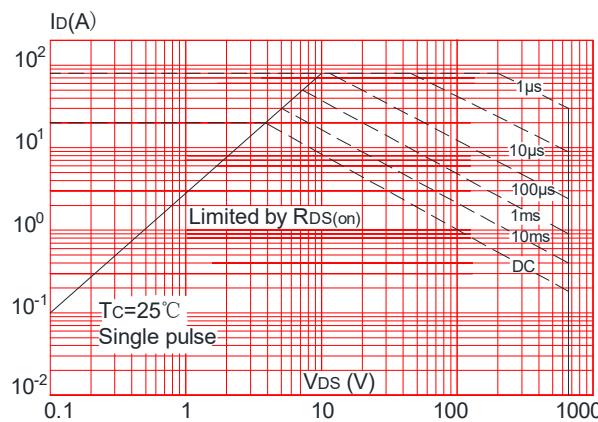


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

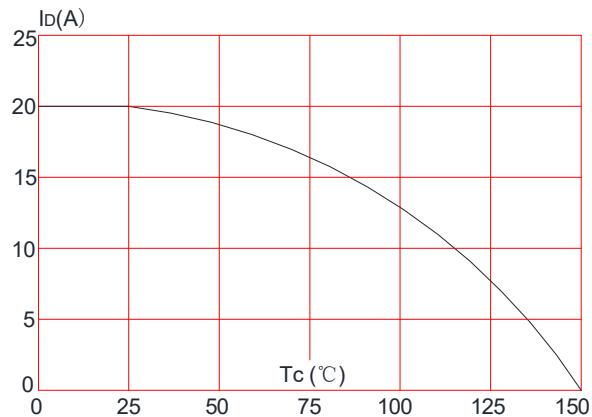
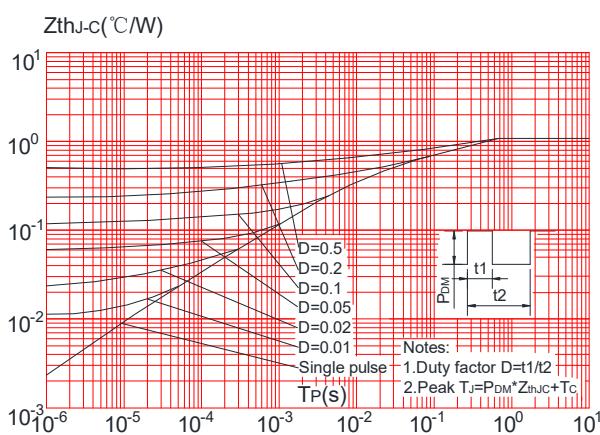


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit



Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

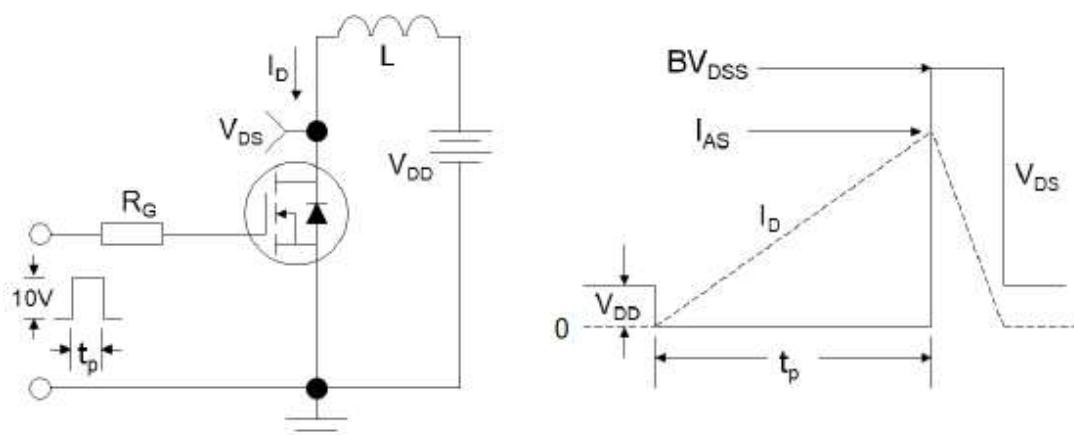
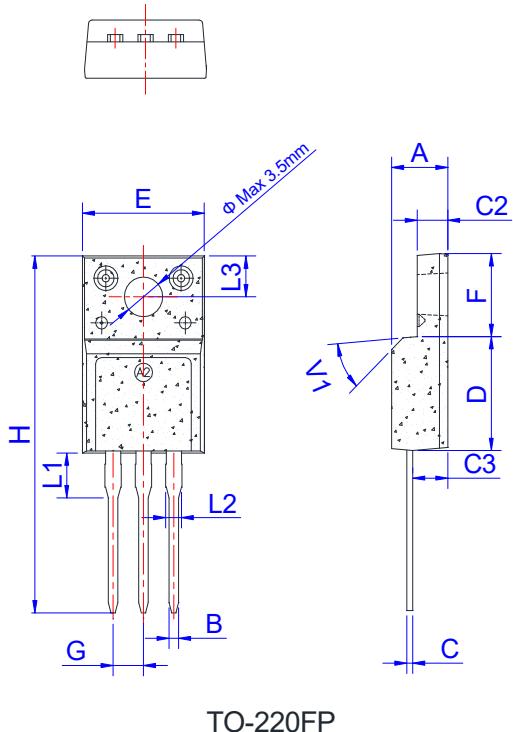


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-TO-220FP



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.50		4.90	0.177		0.193
B	0.74	0.80	0.83	0.029	0.031	0.033
C	0.47		0.65	0.019		0.026
C2	2.45		2.75	0.096		0.108
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.80		10.4	0.386		0.410
F	6.40		6.80	0.252		0.268
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.63			0.143	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	

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