



Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

- 60V, 50A
- $R_{DS(ON)} < 12m\Omega$ @ $V_{GS} = 10V$
- $R_{DS(ON)} < 16m\Omega$ @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

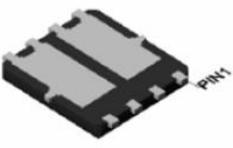
- Load Switch
- PWM Application
- Power management



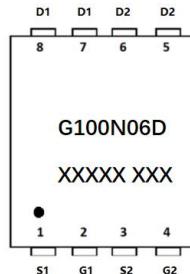
100% UIS TESTED!
100% ΔV_{ds} TESTED!



Top View

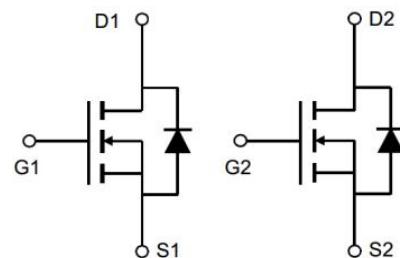


Bottom View



PDFN5X6-8L(Dual)

Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
G100N06D	JMTG100N06D	TAPING	PDFN5X6-8L	13inch	2500	25000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	50	A
		$T_C = 100^\circ C$	33	A
I_{DM}	Pulsed Drain Current ^{note1}		200	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		100	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	51	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.5	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	1.7	2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	9.5	12	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$	-	11.5	16	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	4605	-	pF
C_{oss}	Output Capacitance		-	215	-	pF
C_{rss}	Reverse Transfer Capacitance		-	191	-	pF
Q_g	Total Gate Charge	$V_{DS}=30\text{V}$, $I_D=20\text{A}$, $V_{GS}=10\text{V}$	-	77	-	nC
Q_{gs}	Gate-Source Charge		-	9	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	23	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30\text{V}$, $I_D=30\text{A}$, $R_G=1.8\Omega$, $V_{GS}=10\text{V}$	-	7.1	-	ns
t_r	Turn-on Rise Time		-	5.3	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	27.2	-	ns
t_f	Turn-off Fall Time		-	6.2	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	50	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	200	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s=30\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=30\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	29	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	45	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : $T_J=25^\circ\text{C}$, $V_{DD}=30\text{V}$, $V_G=10\text{V}$, $L=0.5\text{mH}$, $R_g=25\Omega$, $I_{AS}=20\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

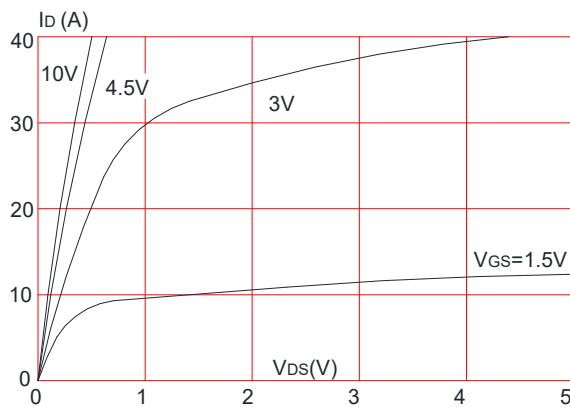


Figure 3: On-resistance vs. Drain Current

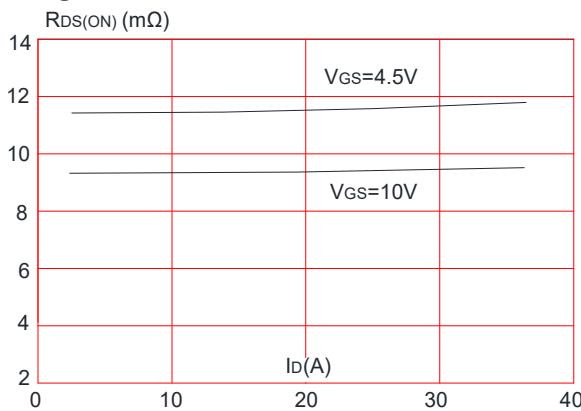


Figure 5: Gate Charge Characteristics

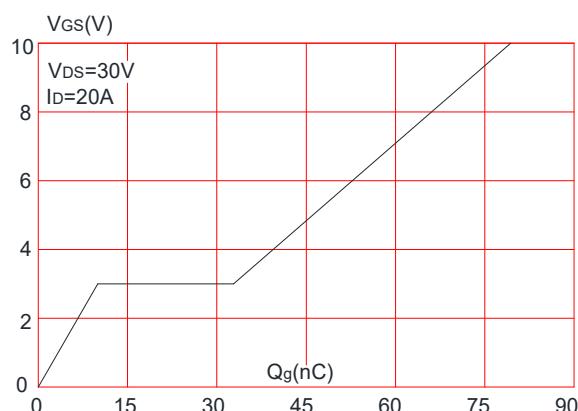


Figure 2: Typical Transfer Characteristics

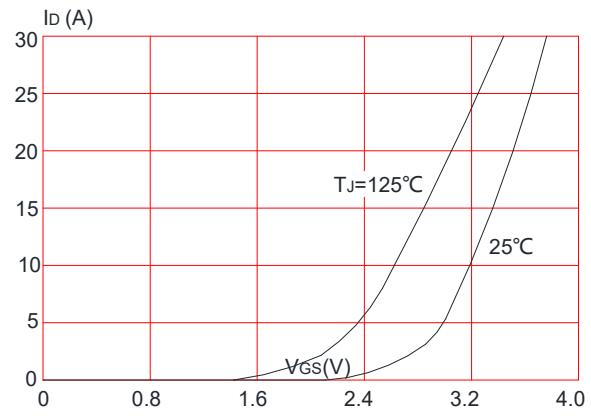


Figure 4: Body Diode Characteristics

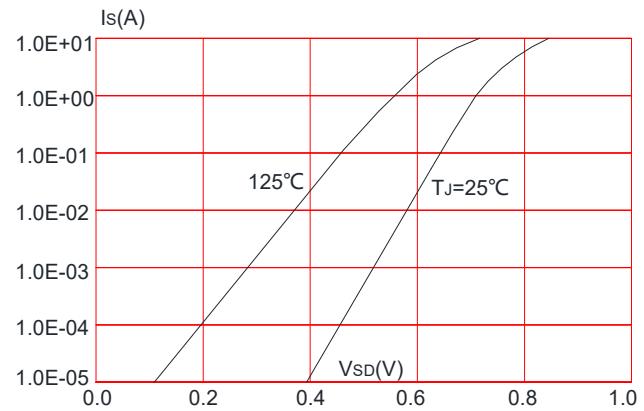


Figure 6: Capacitance Characteristics

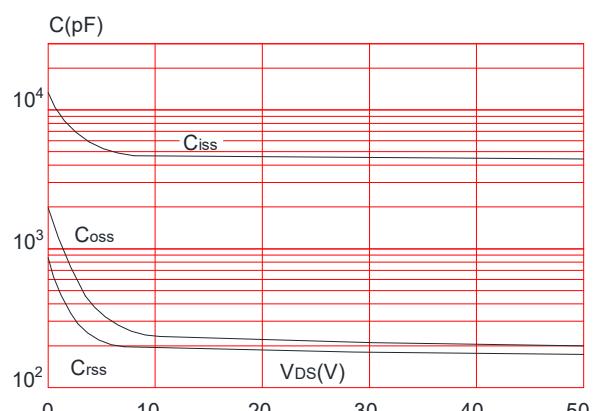


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

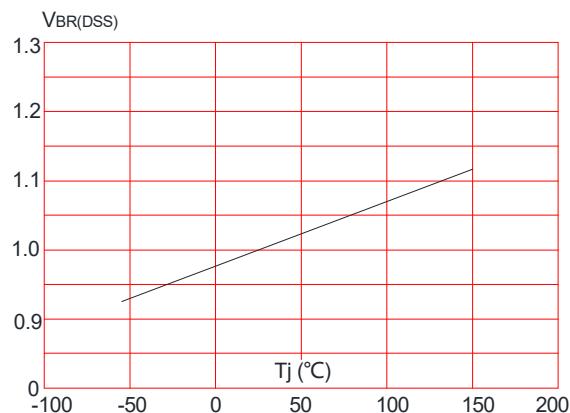


Figure 8: Normalized on Resistance vs. Junction Temperature

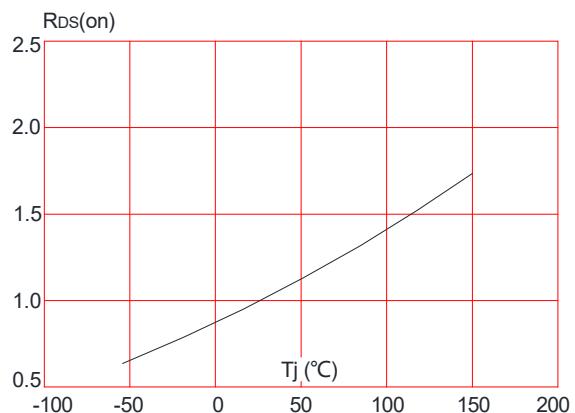


Figure 9: Maximum Safe Operating Area

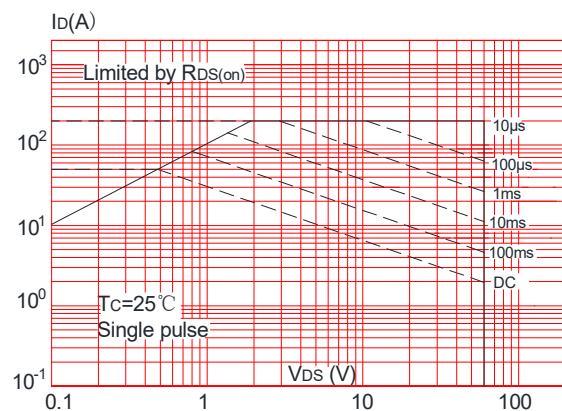


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

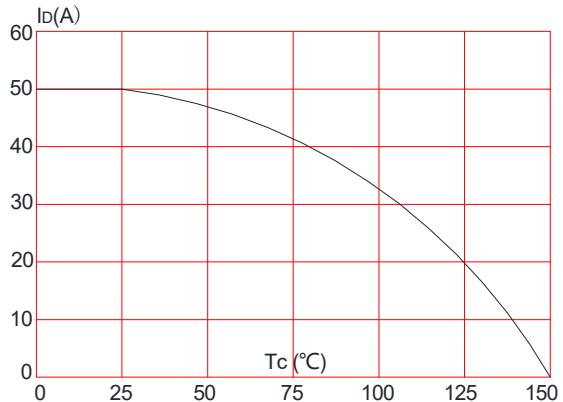
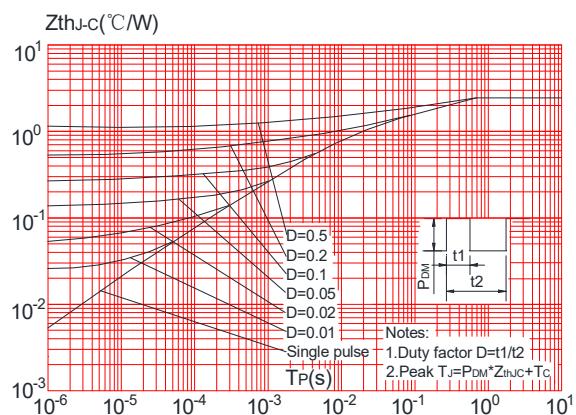


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

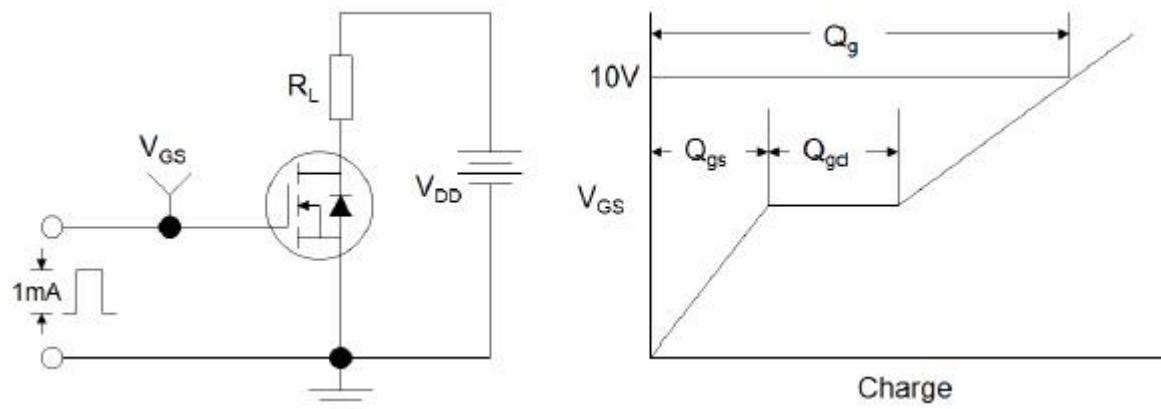


Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

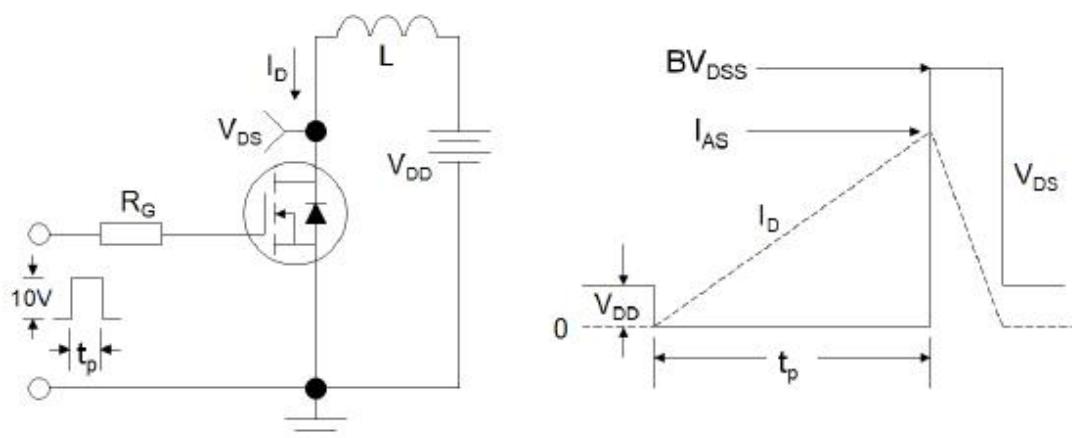
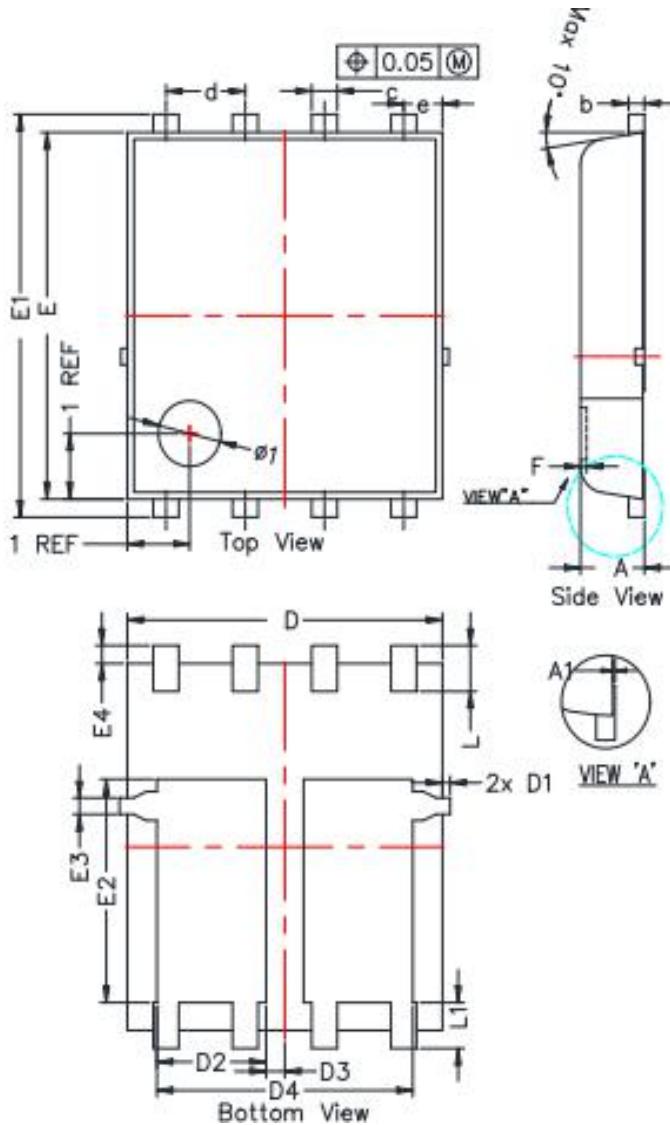


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data- PDFN5X6-8L



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	—	0.050	0.000	—	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d	1.27 BSC			0.050 BSC		
* D	4.950	5.050	5.150	0.195	0.199	0.203
*D1	—	—	0.125	—	—	0.005
*D2	1.650	1.750	1.850	0.065	0.069	0.073
D3	0.200	0.300	0.400	0.008	0.012	0.016
D4	4.000	4.100	4.200	0.157	0.161	0.165
e	0.62 BSC			0.024 BSC		
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.310	3.410	3.510	0.130	0.134	0.138
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
* L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.
Copyright ©2021 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.